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Design and Development of Control System using Atmel 89c51ED2/RD2.

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Abstract

In this paper, we designed and implemented a microcontroller-based Control system *using Atmel AT89c51ED2/RD2.* The system has additional external interfaces such as ADC, SRam, Flash, UART, and LCD display. The system consists of two sets of modules i.e, alarm module and controller module. The experiment results show that our system works as expected.

Keywords--- ADC, Flash, Microcontroller, SRam, UART.

Introduction

Controller is a device, in the form of a chip, analogue electronics, or computer, which monitors and physically alters the operating conditions of a given dynamical system. The system here is MIMO that is multiple input multiple outputs. The paper consists of designing and development of trip modules, for controlling application. Trip module consists of two sets of boards, alarm board, controller board, and master control for remote application. Controller board mainly consists of microcontroller At89c51RD2/ED1 [3], ADC, SRam, Flash, uart, and LCD display. Controller board receives input from the residual board and generates control signal to alarm board and display message through LCD display.

Microcontroller (AT89C51RD2/ED2)

AT89C51RD/2ED2 is high performance CMOS Flash version of the 80C51 CMOS single chip 8-bit microcontroller [3],[4]. It contains a 64-Kbyte Flash memory block for code and for data. The 64-Kbytes Flash memory can be programmed either in parallel mode or in serial mode with the ISP capability or with software. The programming voltage is internally generated from the standard VCC pin. The AT89C51RD2/ED2 retains all of the features of the Atmel 80C52 with 256 bytes of internal RAM, a 9-source 4-level interrupt controller and three timer-counters. The AT89C51ED2 provides 2048 bytes of EEPROM for nonvolatile data storage. In addition, the AT89C51RD2/ED2 has a Programmable Counter Array, an XRAM of 1792bytes, a Hardware Watchdog Timer, SPI interface, Keyboard, a more versatile serial channel that facilitates multiprocessor communication (EUART) and a speed improvement mechanism (X2 Mode).

Flash Memory (SST39SF010A)

The SST39SF010A/020A/040 is CMOS Multi-Purpose Flash (MPF) manufactured with SSTs proprietary, high performance CMOS Super Flash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A/020A/40 devices write (Program or Erase) with a 4.5-5.5V power supply [7].

SRAM (CY62128ELL-45ZXA)

The CY62128E is a high performance CMOS static RAM organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling [8].

UART (NS16C2752)

UART (Universal Asynchronous Receiver and Transmitter) is a device allowing the reception and transmission of information, in a serial and asynchronous way. A UART allows the communication between a computer and several kinds of devices (printer, modem, etc), interconnected via an RS-232 cable. In this project we use UART for serial transmission [9].

ADC (AD7654)

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device that converts a continuous quantity to a discrete time digital representation. An ADC may also provide an isolated measurement. Typically, an ADC is an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. ADC used in this project is AD7654 which is a low cost, simultaneous sampling, dual channel, 16 bit, charge redistribution SAR, analog to digital converter that operates from a single 5 V power supply [10].

LINE DRIVER (74HC244)

The 74HC244 is a high speed Si gate CMOS device and is pin compatible with Low power Schottky TTL (LSTTL). The 74HC244; 74HCT244 has octal non-inverting buffer line drivers with 3 state outputs. The 3 state outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on OE causes the outputs to assume a high impedance OFF-state. 74HCT244 is identical to the 74HC240; 74HCT240 but has non-inverting outputs [13].

Optocouplers(HCPL2731)

HCPL2730/HCPL2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split Darlington photo detector. The split Darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler [15].

Controller Module Architecture

Requirement specification

I. Power supply: 24v dc power supply
II. Current : 4-20 mA
III. Digital input : 36 no.(D0-D35)
IV. Analog input : Iso-analog-parameter
V. Digital output :mux-en-1, mux-en2,A0,A1,A2
VI. UART Interface
VII. LCD Interface
VIII. ADC Interface
IX. Memory interface: There are two memory interfaces involved they are

- RAM Interface
- Flash Interface

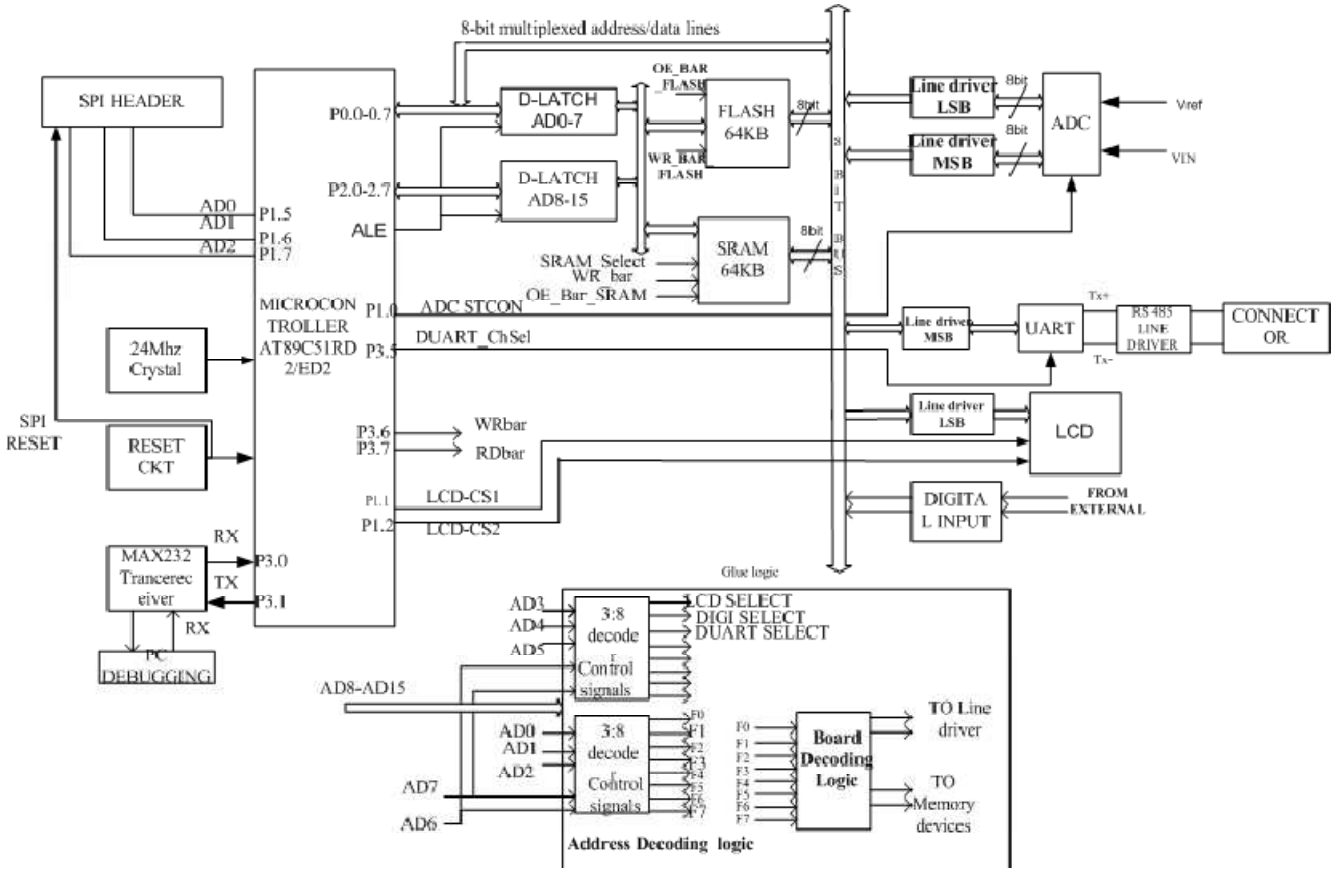


Fig1.Block Diagram of Controller module Architecture

The Block Diagram of Controller module mainly consists of microcontroller At89c51RD2/ED1, ADC, SRAM, Flash, UART, LCD display and MAX232 and glue logic circuitry providing control inputs to all the circuit elements. Controller module receives analog input Iso-analog-parameter from the residual boards ,it is converted to digital signal from the ADC AD7654 it is converted to 16-bit digital signal ,through which two 8-bit LSB and MSB are fed to the microcontroller data bus through line driver on the reception of data signals microcontroller does the action dependent on the corresponding signal and its displayed through LCD display from the specification shown in the 3.1 ,i have drawn the block diagram of controller module architecture as
shown in figure1 using MS Visio .Schematics are drawn using orcad capture cis. Bill of materials which consists of circuit
Reference, Component Description/Specification, Ordering Part , Manufacturer Name, quantity, package, operating temperature .
Block diagram consists of external interfaces such as FLASH, SRAM, UART, Digital inputs and glue logic circuit providing control signal for each device to enable or disable.

Glue logic

Glue logic is the custom logic circuitry used to interface a number of off the-shelf integrated circuits. This is often achieved using ordinary series components. In more complex cases, programmable logic devices like a CPLD or FPGA might be used. The falling price of programmable logic de-
vices, combined with their reduced size and power consumption (compared to discrete components), is making them common even for simple systems.
Typical functions of glue logic may include (but not limited to):
1. Simple logic functions.
2. Address decoding circuitry used with older processors like the 6502 or Z80 to divide up the processor's address space into RAM, ROM and I/O. Newer versions of these processors (such as 65816 or eZ80), may add features that enable glueless interfacing to external devices.
3. Buffers to protect outputs from overload, or protect sensitive inputs from ESD damage.
4. Voltage level conversion, e.g. when interfacing one logic family (CMOS) to another (TTL).
5. Programmable logic can be used to hide the exact function of a circuit, in order to prevent a product from being cloned or counterfeited The figure below shows the block diagram of Glue logic which is used to generate control signals for various circuit components such as RAM, LCD, ADC, DUART and for address decoding circuitry.

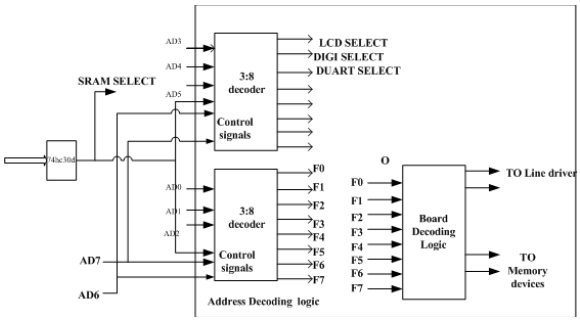


Figure 2: Block diagram of Glue logic

The following are the tests carried on the controller module are as follows:

A. Bare board test

After PCB fabrication is done, we need to do the bare board test before placing the components on board. bare board test include
i. testing the continuity between the each and every circuit components as in the net list shown in Appendix B
ii. Testing for short circuit between vcc and ground
iii. Testing for isolation between the different grounds

B. Tests on Power Supply Circuit

The power supply circuit takes 24V as input and generates isolated three sets of +5, +/-15V power supplies.

C. Power on Tests

After placing the components on board, we need to check whether proper voltage is generated, as by applying 24V as input power supply through 14 Pin Rack and Panel connector and we need to check expected and observed voltages at test pointsand we need to note down the following values. Read-
ings of the voltages for TP1, TP2 and TP3 shall be with respect to TP4.Readings of the voltages for TP5, TP6 and TP7 shall be with respect to TP8.Readings of the voltages for TP9, TP10 and TP11 shall be with respect to TP12.

D. Load Regulation Tests

Load regulation: It is the capability to maintain a constant voltage (or current) level on the output channel of a power supply despite changes in the resistor's load.
There are three sets of isolated power supplies generated by U57, U58 and U59 Connect load as shown in test setup to 5V supply of U57 through J3 and change load from 25 % of full load to maximum load as shown in fig.3and note down the voltage reading .Connect load as shown in test setup to 15V supply of U57 through J3 and change load from 25 % of full load to maximum load as shown in figure4 and note down the voltage reading .Connect load as shown in test setup to -15V supply of U57 through J3

and change load from 25 % of full load to maximum load and note down the voltage reading .
Connect load as shown in test setup to 5V supply of U58 through J3 and change load from 25 % of full load to maximum load shown in fig.4 and note down the voltage reading .Connect load as shown in test setup to 15V supply of U58 through J3 and change load from 25 % of full load to maximum load shown in fig.5 and note down the voltage reading .Connect load as shown in test setup to -15V supply of U58 through J3 and change load from 25 % of full load to maximum load and note down the voltage reading .Connect load as shown in test setup to 5V-MCR supply of U59 through J3 and change load from 25 % of full load to maximum load and note down the voltage reading .Connect load as shown in test setup to 15V-MCR supply of U59 through J3 and change load from 25% percentage of full load to maximum load and note down the voltage reading tabulated in table 5.9 Connect load as shown in test setup to -15V-MCR supply of U59 through J3 and change load from 25% percentage of full load to maximum load and note down the voltage reading .Now connect the load at 15V of U57 and repeat the experiment.

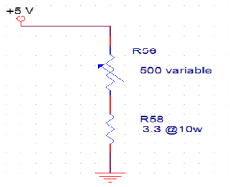


Figure 3: simulation circuit for load regulation across 5v power supply

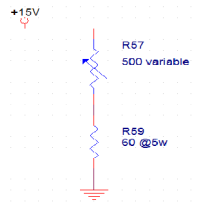


Figure 4: simulation circuit for load regulation across 15v power supply

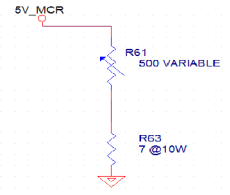


Figure 5: simulation circuit for load regulation across 5v MCR power supply.

E. Line Regulation Tests

Line Regulation: Line Regulation is the capability to maintain change in output voltage level of power supply despite the change in input voltage.
In this test the input 24V power supply shall be varied from minimum 9 V to maximum 36V and output voltages at TP1, TP2, TP3, TP5, TP6, TP7, TP9,TP10 and TP11 shall be monitored and readings shall be noted for minimum to maximum voltage observed at above mentioned test points.

Experimental Results

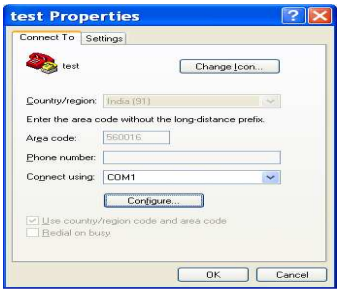
The result of my paper goes in several phases; firstly design of schematics from the specification document using Or cad capture cis. Secondly Gerber verification was done by checking each and every component layout specification given in respective product data sheet. after pcb fabrication, bare board test is carried to check any short between vcc and ground ,continuity between each and every components respectively which is done on the bare board .next assembly of components is done, then power on test, line regulation test and load regulation test is carried. During power on test we are Checking expected voltage and observed voltage at various test points and at the power connector J3.the expected and observed voltage. During load regulation test, checking capability to maintain a constant voltage level on the output channel of a power supply despite changes in the resistor's load. As there are three sets of voltages generated in the cir-cuit we need to perform load regulation for each and every voltage source. During line regulation test checking capability to maintain a constant voltage level on the output channel of a power supply despite changes in the resistor's load. Figure6 shows the Snapshot Top view of controller module with assembled components.Figure7 shows the snapshot of downloading cable for controller module.

Figure6: Snapshot Top view of controller module with assembled components.

Figure 5.5: Snapshot of Downloading Cable for controller board

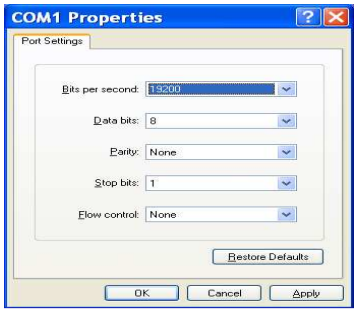
A. Configuration details

RS-232 Communication Configuration
Select the COM Port



Configure the parameter as shown below

Baud Rate	19200bps
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None



Conclusion And future Work

Controller module for which is designed to receive input from the residual board and generates control signal to alarm board and display message through LCD display. power on test is carried on the board provides satisfactory voltages at various test points. the expected and observed voltage at various test points, resembling the same voltage across various test points.

Load regulation test performed on the board gives desired results such that maintaining a constant voltage on the output channel of a power supply despite changes in the resistor's load. Line regulation test performed on the board gives desired results such that maintaining change in output voltage level of power supply despite the change in input voltage. line regulation test results which shows expected voltage for different set of input voltage from 9v-32v respectively. thus all the tests on the board are proven so the board can be interfaced with residual board for controlling application. Developed controller module shall be interfaced with alarm board, the combination of the module will result in alarming the system.

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